CLAIMS

What is claimed is:

1. A photodetecting array comprising:

a plurality of detecting cells arranged in an array;

a staircase grid of bias lines coupled to said plurality of detecting cells;

a plurality of gate lines coupled to said plurality of detecting cells; and

a plurality of data lines coupled to said plurality of detecting cells.

2. A photodetecting array as in claim 1 wherein each of said plurality of detecting cells comprises a transistor and a photodiode, and wherein one of said plurality of gate lines is coupled to said transistor and one of said plurality of data lines is coupled to said transistor.

3. A photodetecting array as in claim 2 wherein said photodiode comprises:

an n+ layer formed over a first passivation layer;

an amorphous silicon layer formed over said n+layer;

a p+layer formed over said amorphous silicon layer; and

a conductive layer formed over said p+layer.

4. A photodetecting array as in claim 2 wherein each photodiode in said array is segmented from other photodiodes in said array.

5. A photodetecting array as in claim 4 wherein said photodiode in a cell is disposed above said transistor in said cell.

6. A photodetecting array as in claim 2 wherein said staircase grid comprises:

a first bias line parallel to a first gate line of said plurality of gate lines;

a second bias line parallel to a second gate line of said plurality of gate lines;

a third bias line parallel to a first data line of said plurality of data lines, said third bias line being electrically coupled between said first bias line and said second bias line.

7. A photodetecting array as in claim 5 wherein said staircase grid comprises:

a first bias line parallel and proximate to a first gate line of said plurality of gate lines;

a second bias line parallel and proximate to a second gate line of said plurality of gate lines;

a third bias line parallel to and adjacent to a first data line of said plurality of data lines, said third bias line being electrically coupled between said first bias line and said second bias line.

8. A photodetecting array as in claim 7 wherein each said photodiode comprises:

a n+layer formed over a first passivation layer;

an amorphous silicon layer formed over said n+layer;

a p+layer formed over said amorphous silicon layer; and

a conductive layer formed over said p+layer.

9. A photodetecting array as in claim 1 wherein said staircase grid comprises a first plurality of bias lines which are parallel to and proximate to corresponding gate lines and a second plurality of bias lines which are parallel to and proximate to only a portion of said plurality of data lines, said second plurality of bias lines being coupled electrically between said first plurality of bias lines.

10. A photodetecting array as in claim 9 wherein a capacitive coupling between said second plurality of bias lines and said plurality of data lines is limited substantially to said portion.

11. A photodetecting device comprising:

a first row of detecting cells, each having a transistor and a photodiode;

a second row of detecting cells, each having a transistor and a photodiode, said second row being adjacent to and parallel with said first row;

a first gate line coupled to said first row;

a second gate line coupled to said second row;

a first bias voltage line parallel with and proximate to said first gate line and coupled to detecting cells in said first row;

a second bias voltage line parallel with and proximate to said second gate line and coupled to detecting cells in said second row.

12. A photodetecting device as in claim 11 wherein said first and said second bias voltage lines provide a reverse bias voltage to photodiodes in said first row of detecting cells and in said second row of detecting cells.

13. A photodetecting device as in claim 11 further comprising:
a third bias voltage line parallel with and proximate to a first data line, said third bias voltage line being electrically coupled between said first bias voltage line and said second bias voltage line.

14. A photodetecting device as in claim 13 further comprising:
a second data line;
a fourth bias voltage line parallel with and proximate to said second data line, said fourth bias voltage line being electrically coupled to said second bias voltage line and to a fifth bias voltage line.

15. A photodetecting device as in claim 14 wherein said first data line and said second data line are substantially perpendicular to said first gate line and to said second gate line and wherein said third bias voltage line is not coupled to said fifth bias voltage line and wherein said fourth bias voltage line is not coupled to said first bias voltage line.

16. A photodetecting device as in claim 15 wherein said first gate line is coupled to transistors in said first row of detecting cells and said second gate line is coupled to transistors in said second row of detecting cells.

17. A photodetecting device as in claim 11 wherein each photodiode in said first row and in said second row of detecting cells is segmented from other photodiodes.

18. A photodetecting device as in claim 17 wherein said photodiode in a cell is disposed above said transistor in said cell.

19. A photodetecting device as in claim 18 wherein each said photodiode comprises:

an n+layer formed over a first passivation layer;

an amorphous silicon layer formed over said n+layer;

a p+layer formed over said amorphous silicon layer; and

a conductive layer formed over said p+layer.

20. A photodetecting array comprising:

a plurality of detecting cells arranged in an array, each of said detecting cells comprising a photodiode;

a plurality of gate lines coupled to said plurality of detecting cells;

a plurality of data lines coupled to said plurality of detecting cells;

a mesh of bias voltage lines, said mesh comprising first bias lines disposed in a first direction which is substantially parallel to said gate lines and second bias lines disposed in a second direction which is substantially perpendicular to said gate lines and wherein a total length of said first bias lines exceeds a total length of said second bias lines.

21. A photodetecting array as in claim 20 wherein said total length of said first bias lines greatly exceeds said total length of said second bias lines by a factor of at least 10 times, and wherein said first bias lines are proximate to corresponding said gate lines.

22. A method for manufacturing a photodetecting array, said method comprising:

forming a plurality of detecting cells arranged in an array, each of said detecting cells comprising a photodiode;

forming a plurality of gate lines coupled to said plurality of detecting cells;

forming a plurality of data lines coupled to said plurality of detecting cells;

forming a mesh of bias voltage lines, said mesh comprising first bias lines disposed in a first direction which is substantially parallel to and proximate to said gate lines and second bias lines disposed in a second direction which is substantially perpendicular to said gate lines and wherein a total length of said first bias lines exceeds a total length of said second bias lines.

23. A photodetecting array comprising:

a plurality of detecting cells arranged in an array, each of said detecting cells having a photodiode and a transistor;

a plurality of gate lines coupled to said plurality of detecting cells;

a plurality of data lines coupled to said plurality of detecting cells;

a plurality of bias voltage lines, each of said bias voltage lines having at least a pixel defect correcting portion which couples said each bias voltage line to a corresponding photodiode, said pixel defect correcting portion capable of disconnecting said bias voltage line from said corresponding photodiode.

24. A photodetecting array as in claim 23, wherein said corresponding photodiode occupies most of an area of its corresponding detecting cell except for said pixel defect correction portion.

25. A photodetecting array as in claim 23, wherein said bias voltage lines provide a reverse bias voltage to each of said photodiodes.

26. A photodetecting array as in claim 25 wherein said pixel defect correcting portion is formed by making the electrode, which connects said bias voltage line to said corresponding photodiode, thinner than adjacent electrodes.

27. A photodetecting array as in claim 25 wherein each said photodiode is formed above each said transistor and wherein said bias voltage lines are formed above said photodiode.

28. A photodetecting array as in claim 27 wherein each said photodiode in said array is segmented from other photodiodes in said array.

29. A photodetecting array as in claim 28 wherein said plurality of bias voltage lines are formed in a mesh which comprises first bias lines disposed in a first direction which is substantially parallel to said gate lines and second bias lines disposed in a second direction which is substantially perpendicular to said gate lines and wherein a total length of said first bias lines exceeds a total length of said second bias lines.